DELAY LOCKED LOOP FOR IMPROVING HIGH FREQUENCY CHARACTERISTICS AND YIELD

ABSTRACT OF THE DISCLOSURE

A delay locked loop (DLL) is provided that generates an internal clock signal in synchronization with an external clock signal. First through third amplifiers convert the swing width of the external clock signal to a small swing width and re-convert the external clock signal to an external signal level. A basic clock generator generates a plurality of basic clock signals that are progressively shifted apart by a predetermined phase. First through third duty correctors correct the external clock signal, a first internal clock signal, and a second internal clock signal to satisfy 50% duty. First and second mixers generate a first clock signal and a second clock signal which is 90 degrees out-of-phase with the first clock signal. Finally, the first internal clock signal is 90 degrees out-of-phase with the second internal clock signal. Thus, the first internal clock signal is synchronous with the external clock signal.